The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method for manufacturing a semiconductor device comprising the steps of:

forming an interlayer insulator comprising at least an upper layer comprising silicon nitride and a lower layer comprising silicon oxide, each comprising different dry etching characteristics;

etching the upper layer of the interlayer insulator using a first mask, wherein the lower layer of the interlayer insulator is used as an etching stopper;

forming a second mask to cover a portion of the lower layer of the interlayer insulator, which is exposed by the etching step; and

selectively etching the lower layer of the interlayer insulator using the second mask to form a contact hole,

wherein the second mask is different from the first mask.

2. (Previously Presented) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator comprising at least two layers on the gate insulating film;

forming a first contact hole by removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region, wherein the lower layer of the interlayer insulator is used as an etching stopper;

forming a second contact hole overlapped with the first contact hole through the interlayer insulator to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

3. (Previously Presented) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film comprising aluminum on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator comprising at least two layers on the gate insulating film;

forming a first contact hole by removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region, wherein the lower layer of the interlayer insulator is used as an etching stopper;

forming a second contact hole overlapped with the first contact hole through the interlayer insulator to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

4. (Previously Presented) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator comprising at least two layers on the gate insulating film;

forming a first contact hole by removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region, wherein the lower layer of the interlayer insulator is used as an etching stopper;

forming a second contact hole overlapped with the first contact hole to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode,

wherein the second contact hole is formed smaller than the part.

5. (Previously Presented) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator on the gate insulating film;

forming a first contact hole by removing a part of the interlayer insulator, the part being located over at least one of a source region and a drain region, wherein a part of the interlayer insulator located under the first contact hole is used as an etching stopper;

forming a second contact hole overlapped with the first contact hole through the interlayer insulator to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

6. (Canceled)

7. (Original) The method according to claim 2 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

8. (Original) The method according to claim 3 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

9. (Original) The method according to claim 4 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

10. (Original) The method according to claim 5 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

11. (Original) The method according to claim 2 wherein the pixel electrode comprises indium tin oxide.

12. (Original) The method according to claim 3 wherein the pixel electrode comprises indium tin oxide.

13. (Original) The method according to claim 4 wherein the pixel electrode comprises indium tin oxide.

14. (Original) The method according to claim 5 wherein the pixel electrode comprises indium tin oxide.

15. (Original) The method according to claim 2 wherein the gate electrode is anodized.

16. (Original) The method according to claim 3 wherein the gate electrode is anodized.

17. (Original) The method according to claim 4 wherein the gate electrode is anodized.

18. (Original) The method according to claim 5 wherein the gate electrode is anodized.

19. (Original) The method according to claim 1 wherein the semiconductor device is a liquid crystal display device.

20. (Original) The method according to claim 2 wherein the semiconductor device is a liquid crystal display device.

21. (Original) The method according to claim 3 wherein the semiconductor device is a liquid crystal display device.

22. (Original) The method according to claim 4 wherein the semiconductor device is a liquid crystal display device.

23. (Original) The method according to claim 5 wherein the semiconductor device is a liquid crystal display device.

24. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a wiring line;

forming a first interlayer insulating film over the thin film transistor and the wiring line;

forming a second interlayer insulating film on the first interlayer insulating film wherein the second interlayer insulating film has a different etching characteristic from the first interlayer insulating film;

forming a first opening and a second opening in the second interlayer insulating film by first etching to expose a surface of the first interlayer insulating film wherein the first interlayer insulating film functions as an etching stopper during the first etching;

forming a third opening in the first interlayer insulating film by second etching the exposed surface of the first interlayer insulating film; and

forming an electrode in the second opening over the wiring line with the first interlayer insulating film interposed therebetween,

wherein a thickness of the ~~second~~ first interlayer insulating film is 1/5 to 1/50 of a total thickness of the first interlayer insulating film and the second interlayer insulating film.

25. (Previously Presented) The method according to claim 24 wherein the first interlayer insulating film comprises silicon oxide and the second interlayer insulating film comprises silicon nitride.

26. (Previously Presented) The method according to claim 24 wherein the semiconductor device is a liquid crystal device.

27. (Previously Presented) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a semiconductor island on an insulating surface;

forming a gate insulating film comprising silicon oxide on the semiconductor island;

forming a gate electrode over the semiconductor island with the gate insulating film interposed therebetween;

forming a wiring line over the insulating surface;

forming a first insulating film comprising silicon oxide over the gate insulating film and the gate electrode;

forming a second insulating film comprising silicon nitride on the first interlayer insulating film;

first etching the second insulating film to form a first opening and a second opening wherein the first insulating film functions as an etching stopper;

second etching a portion of the first insulating film and the gate insulating film in accordance with the first opening of the second insulating film, thereby, exposing a surface of the semiconductor layer; and

forming an electrode in the second opening over the wiring line with the first insulating film interposed therebetween,

wherein a thickness of the second interlayer insulating film is 1/5 to 1/50 of a total thickness of the first interlayer insulating film and the second interlayer insulating film.

28. (Previously Presented) The method according to claim 27 wherein the semiconductor device is a liquid crystal device.

29. (Previously Presented) The method according to claim 1,

wherein at least a first opening and a second opening are formed in the upper layer of the interlayer insulator by etching the upper layer of the interlayer insulator using a first mask,

wherein the first opening is overlapping the portion of the lower layer of the interlayer insulator, and

wherein the second opening is covered by the second mask in selectively etching the lower layer of the interlayer insulator.

30. (Previously Presented) The method according to claim 1, wherein a part of an upper surface of the lower layer of the interlayer insulator is exposed in the contact hole.